REMARKS

Claims 1-11, and 13-33 are currently pending in this application. Claims 10, 11, and 13-33 have been allowed. Claims 2, 4, and 7 were objected to as being dependent upon a rejected base claim, but the Examiner has indicated that they would be allowable if rewritten in independent form, including parent limitations. Applicants have amended claims 2 and 7 in independent form including parent limitations, and therefore submit that the claims are now in condition for allowance. Claims 1, 3, 5, 6, 8 and 9 stand rejected under 35 U.S.C. §103. Reconsideration and further examination of the rejected claims is respectfully requested for the reasons provided below.

Rejections under 35 U.S.C. §102(e)

Claims 1, 3, 5, 6, 8 and 9 were rejected under 35 U.S.C. §103 as being unpatentable over Hershey et al (U.S. Patent 6,167,062).

Hershey, U.S. Patent 6,167,062

Hershey addresses the problems of payload mapping, stating "The essence of the payload mapping process is to synchronize the tributary signal with the envelope capacity provided for transport. This is achieved by adding extra stuffing bits (also called justification bits) to the STS-1 signal bit stream as part of the mapping process. For example, a DS3 tributary signal at a nominal rate of 44 Mbps needs to be synchronized with an envelope capacity of 51.840 Mbps (minus STS path overhead). In such manner an, asynchronous low bandwidth payload is embedded within a high bandwidth multiplexed synchronous signal..." (Col. 1 lines 38-53). Hershey states that before Hershey's invention "it was not easy to reliably retrieve the

asynchronous timing relationships between individual payloads subsequent to the signal processing function..."

Hershey describes "... System modules are provided for connection to a telecommunications network. The modules demultiplex asynchronous payloads, synchronize them, process them, and then restore their asynchronous relationships..." (col. 2, lines 9-13). At column 4. lines 62-68 through column 5, lines 2, Hershey describes:

"... The control and management memory and circuitry module 130a includes . . programmable hardware such as Field Programmable Gate Arrays (FPGA) which permit dynamic configuration of the network interface section 30 in accordance with network performance parameters, or though operator supplied modifications. In this way, the architecture of the network interface board is not limited by either the network protocol or the physical connection, but is reconfigurable through the control and management memory and circuitry..."

In order to support a rejection under 35 U.S.C. §102, *every* limitation in the claims should be shown or suggested by the references. Applicants submit that this burden is not met through the application of the Hershey reference.

For example, claim 1 recites "..."...A transparent port for a high rate network comprising ... a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and *extracting a user signal and a data clock* ... a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol..."

In contrast, Hershey describes, at column 6, line 25 "The SMC section 50 uses a 'fast clock' signal to synchronize the plurality of asynchronous payloads..." Such an arrangement if

fundamentally different than that recited in the claims. In addition, Applicants note that, in the office action of February 27, 2003, the Examiner stated, at page 3 "Hershey is silent on transparent system with a receiver that extracts data signals and data clock..." Accordingly, for at least the reason that Hershey neither describes nor suggests all the elements of claim 1, the rejection under 35 U.S.C. §102(e) is improper and should be withdrawn.

Claims 3, 5, 6, 8 and 9 depend on claim 1, add further patentable limitations to claim 1, but are allowable for at least the reasons discussed with regard to claim 1.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Lindsay McGuinness, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

12/1/2003
Date

Lindsay McGuinness, Reg. No. 38,549
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
30 Nagog Park Drive
Acton, MA 01720
(978) 264-6664

Docket No. 10799ROUS01U 120-219
Dd: 12/3/2003

MARKED-UP CLAIMS

1. (original) A transparent port for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol.

2. (Currently amended) A transparent port for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol ~~as claimed in claim 1,~~ wherein said PLT translates said user signal into a data signal whenever said rate R1 corresponds to a provisioned first protocol and passes said user signal unchanged whenever said rate R1 is not recognized by said processing unit.

3. (original) A transparent port as claimed in claim 1, wherein said PLT performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

4. (original) A transparent port as claimed in claim 2, further comprising a mapping unit for rearranging the bits of said data signal into a container signal of a rate R corresponding to a second protocol.

5. (original) A transparent port as claimed in claim 1, wherein said PLT comprises logic gates configured to perform measurement of a provisioned parameter.

6. (original) A transparent port as claimed in claim 1, wherein said PLT is a programmable gate array.

7. (Currently amended) A transparent port ~~as claimed in claim 1~~ for a high rate network comprising:

a receiver unit for receiving an incoming signal of an arbitrary data rate R1 and extracting a user signal and a data clock;

a programmable link termination PLT for reporting a set of performance parameters for said incoming signal; and

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said incoming signal and configuring said PLT according to said first protocol wherein said set of performance parameters includes a previous section fail indicator.

8. (original) A transparent port as claimed in claim 1,- wherein said set of performance parameters includes one or more of signal strength, clock continuity and jitter.

9. (original) A transparent port as claimed in claim 1, wherein said PLT performs one ore more of a framing, an error count, a code conversion, and a parity correction operation.

10. (Previously Amended) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol;

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; and

a reverse mapping unit for rearranging the bits of a container signal of a second protocol into said data signal of said first protocol.

11. (original) A transparent port as claimed in claim 10, wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

12. (Cancelled).

13. (original) A transparent port as claimed in claim 10, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

14. (original) A transparent port as claimed in claim 10, wherein said PLI is a programmable gate array.

15. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes a previous section fail indicator.

16. (original) A transparent port as claimed in claim 10, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

17. (original) A transparent port as claimed in claim 10, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

18. (original) A method for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network as a transparent tributary, comprising:

at a transmit terminal, selecting a container signal of a rate R, higher than said rate R1;

detecting the rate R1 of said continuous digital signal and determining a first protocol corresponding to said rate R1;

measuring according to a first protocol a set of performance parameters on said continuous signal and reporting said set of performance parameters; and

translating said set of performance parameters from said first protocol to a second protocol characterizing said container signal and providing said translated set into said container signal.

19. (original) A method as claimed in claim 18, further comprising transmitting said container signal from said transmit terminal to a receive terminal.

20. (original) A method as claimed in claim 18, further comprising informing said receive terminal of said rate R1 and of said first protocol through signaling.

21. (original) A method as claimed in claim 20, further comprising:

at the receive terminal, recovering said container signal;

extracting said set of performance parameters from said container signal; and

reconstituting said continuous signal based on said rate R1.

22. (original) A method as claimed in claim 21, further comprising transmitting said continuous signal with said set of performance parameter to a user.

23. (Previously presented) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1';

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol;

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal; wherein said PLI translates said data signal into a user signal whenever said rate R1' corresponds to a provisional first protocol, and passes said data signal unchanged whenever said rate R1 is not recognized by said processing unit.

24. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

25. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI is a programmable gate array.

26. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.

27. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes signal strength, clock continuity and jitter.

28. (Previously presented) A transparent port as claimed in claim 23, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

29. (Previously presented) A transparent port for a high rate network comprising:

a programmable link instigation PLI for reporting a set of performance parameters for a data signal of an arbitrary rate R1', wherein said set of performance parameters includes a previous section fail indicator;

a processing unit for recognizing a plurality of provisioned protocols, selecting a first protocol characterizing said data signal and configuring said PLI according to said first protocol; and

a transmitter unit connected to said PLI for launching an outgoing signal of said first protocol, comprising user information within said data signal.

30. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI comprises logic gates configured to perform measurement of a provisioned parameter.

31. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI is a programmable gate array.

32. (Previously presented) A transparent port as claimed in claim 29, wherein said PLI performs one or more of a framing, an error count, a code conversion, and a parity correction operation.

33. (Previously presented) A transparent port as claimed in claim 23, wherein said set of performance parameters includes a previous section fail indicator.